Code.No: RR410408 | RR | SET-1

IV B.TECH – I SEM EXAMINATIONS, NOVEMBER - 2010
ADVANCED COMPUTER ARCHITECTURE
(COMMON TO ECE, ECC)

Time: 3hours **Max.Marks:80**

Answer any FIVE questions
All questions carry equal marks
- - -

1. a] Distinguish parallel processing at the job level, the task level and the instruction level.
   b] Explain the high order memory interleaving and its addressing scheme. [8+8]

2. a] Classify the pipeline processors according to the levels of processing giving examples of each class.
   b] Describe the throughput of a K-stage pipeline. [8+8]

3. a] What are the parameters that characterized SIMD computers?
   b] What is masking. Explain the masking mechanism. [8+8]

4. a] With an example illustrate the mechanism of data routing in an array processor.
   b] Explain the architecture of PEPE associative processor. [8+8]

5. a] Briefly describe multi-computer and multi processor architecture.
   b] How are multi-port memories organized with fixed priority in multiprocessors? [8+8]

6. a] Describe the static priority algorithm for bus arbitration in multi processors.
   b] Give the structure of $2^3 X 2^3$ delta network. [8+8]

7. a] Compare control flow computers against data flow computers.
   b] Explain any two VLSI arithmetic modules fro matrix computation. [8+8]

8. a] Describe any two special vector instructions of Cyber 205.
   b] Give the Inter CPU communications structure of Cray X-MP system. [8+8]

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Code.No: RR410408 | RR | SET-2

IV B.TECH – I SEM EXAMINATIONS, NOVEMBER - 2010
ADVANCED COMPUTER ARCHITECTURE
(COMMON TO ECE, ECC)

Time: 3hours **Max.Marks:80**

Answer any FIVE questions
All questions carry equal marks
- - -

1. a] What are the parameters that characterized SIMD computers?
   b] What is masking. Explain the masking mechanism. [8+8]

2. a] With an example illustrate the mechanism of data routing in an array processor.
   b] Explain the architecture of PEPE associative processor. [8+8]

3. a] Briefly describe multi-computer and multi processor architecture.
   b] How are multi-port memories organized with fixed priority in multiprocessors? [8+8]

4. a] Describe the static priority algorithm for bus arbitration in multi processors.
   b] Give the structure of $2^3 X 2^3$ delta network. [8+8]

5. a] Compare control flow computers against data flow computers.
   b] Explain any two VLSI arithmetic modules fro matrix computation. [8+8]

6. a] Describe any two special vector instructions of Cyber 205.
   b] Give the Inter CPU communications structure of Cray X-MP system. [8+8]

7. a] Distinguish parallel processing at the job level, the task level and the instruction level.
   b] Explain the high order memory interleaving and its addressing scheme. [8+8]

8. a] Classify the pipeline processors according to the levels of processing giving examples of each class.
   b] Describe the throughput of a K-stage pipeline. [8+8]

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Code.No: RR410408 | RR | SET-3

IV B.TECH – I SEM EXAMINATIONS, NOVEMBER - 2010
ADVANCED COMPUTER ARCHITECTURE
(COMMON TO ECE, ECC)

Time: 3hours **Max.Marks:80**

Answer any FIVE questions
All questions carry equal marks
- - -

1. a] Briefly describe multi-computer and multi processor architecture.
   b] How are multi-port memories organized with fixed priority in multiprocessors? [8+8]

2. a] Describe the static priority algorithm for bus arbitration in multi processors.
   b] Give the structure of $2^3 X 2^3$ delta network. [8+8]

3. a] Compare control flow computers against data flow computers.
   b] Explain any two VLSI arithmetic modules fro matrix computation. [8+8]

4. a] Describe any two special vector instructions of Cyber 205.
   b] Give the Inter CPU communications structure of Cray X-MP system. [8+8]

5. a] Distinguish parallel processing at the job level, the task level and the instruction level.
   b] Explain the high order memory interleaving and its addressing scheme. [8+8]

6. a] Classify the pipeline processors according to the levels of processing giving examples of each class.
   b] Describe the throughput of a K-stage pipeline. [8+8]

7. a] What are the parameters that characterized SIMD computers?
   b] What is masking. Explain the masking mechanism. [8+8]

8. a] With an example illustrate the mechanism of data routing in an array processor.
   b] Explain the architecture of PEPE associative processor. [8+8]

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Code.No: RR410408 | RR | SET-4

IV B.TECH – I SEM EXAMINATIONS, NOVEMBER - 2010
ADVANCED COMPUTER ARCHITECTURE
(COMMON TO ECE, ECC)

Time: 3hours **Max.Marks:80**

Answer any FIVE questions
All questions carry equal marks
- - -

1. a] Compare control flow computers against data flow computers.
   b] Explain any two VLSI arithmetic modules fro matrix computation. [8+8]

2. a] Describe any two special vector instructions of Cyber 205.
   b] Give the Inter CPU communications structure of Cray X-MP system. [8+8]

3. a] Distinguish parallel processing at the job level, the task level and the instruction level.
   b] Explain the high order memory interleaving and its addressing scheme. [8+8]

4. a] Classify the pipeline processors according to the levels of processing giving examples of each class.
   b] Describe the throughput of a K-stage pipeline. [8+8]

5. a] What are the parameters that characterized SIMD computers?
   b] What is masking. Explain the masking mechanism. [8+8]

6. a] With an example illustrate the mechanism of data routing in an array processor.
   b] Explain the architecture of PEPE associative processor. [8+8]

7. a] Briefly describe multi-computer and multi processor architecture.
   b] How are multi-port memories organized with fixed priority in multiprocessors? [8+8]

8. a] Describe the static priority algorithm for bus arbitration in multi processors.
   b] Give the structure of $2^3 X 2^3$ delta network. [8+8]

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